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APPLICATION DATA SHEET

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Title of Invention	A METHOD OF BASE FORMATION IN A BICMOS PROCESS

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TRANSMITTAL

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Title of Invention	A METHOD OF BASE FORMATION IN A BICMOS PROCESS

Application Number :

Date :

First Named Applicant: Peter J. Geiss

Confirmation Number:

Attorney Docket Number: BUR920030152US1

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Submitted By:	Elec. Sign.	Sign. Capacity
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Documents being submitted:	Files
us-request	BUR920030152US1-usrequ.xml
	us-request.dtd
	us-request.xsl
us-assignment	BUR920030152US1-usassn.xml
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Comments

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Description

A METHOD OF BASE FORMATION IN A BICMOS PROCESS

BACKGROUND OF INVENTION

[0001] *Field of the Invention*

[0002] The present invention generally relates to bipolar complementary metal oxide semiconductor (BiCMOS) and PNP/NPN devices and more particularly to an improved device that uses a silicon layer and spacers to separate the emitter from a silicided portion of the structure.

[0003] *Description of the Related Art*

[0004] As the size of transistors continues to decrease, the resistance of the elements used within the smaller devices becomes more important. For example, the resistance of the base in bipolar complementary metal oxide semiconductor (BiCMOS) and PNP/NPN devices dramatically affects the performance of the devices.

SUMMARY OF INVENTION

[0005] This application discloses a method of making bipolar complementary metal oxide semiconductor (BiCMOS) devices. The invention forms a collector and an intrinsic base above the collector. Shallow trench isolation regions are formed adjacent the intrinsic base, and a raised extrinsic base is formed above the intrinsic base. The invention protects a portion of the extrinsic base using a sacrificial mask that is positioned over the center of the extrinsic base. The invention silicides exposed portions of the extrinsic base. This siliciding process leaves a non-silicided portion of the extrinsic base over the center of the intrinsic base. Next, the invention forms an emitter opening through a center of the non-silicided portion of the extrinsic base, forms insulating spacers in the emitter opening, and then forms an emitter in the emitter opening. Before forming the emitter opening, the invention forms an insulator layer above the extrinsic base, wherein the emitter opening is formed through the insulator layer. The spacers separate the emitter from silicided portions of the extrinsic base.

[0006] Before forming the extrinsic base, the invention patterns an insulator over the center of the intrinsic base and epitaxially grows the extrinsic base over the insulator and the

intrinsic base. This process of epitaxially growing the extrinsic base grows polysilicon above the insulator and single crystal silicon above the exposed portions of the intrinsic base. Further, the siliciding process forms the silicided portions of the extrinsic base horizontally adjacent to the non-silicided portion. The spacers in the emitter opening are formed on this insulator.

[0007] This produces a bipolar transistor in bipolar complementary metal oxide semiconductor (BiCMOS) technologies or bipolar-only technologies that has a collector, an intrinsic base above the collector, a raised extrinsic base above the intrinsic base on the sides, an emitter above the intrinsic base; wherein the emitter has a T-shape with a lower section and an upper section that is wider than the lower section, spacers adjacent the lower section of the emitter and an isolation layer beneath the upper section of the emitter, and a silicide layer adjacent the spacers and beneath the upper section of the emitter.

[0008] This structure includes a dielectric structure over the base and beneath the spacers, where the base is wider than the dielectric structure. The spacers separate the emitter from the extrinsic base and comprise insulators. Because it is self-aligned, the silicide is called a salicide.

[0009] The invention also includes a method of making a NPN or PNP transistor. This method forms a lower semiconductor structure having a first-type impurity (e.g., P-type) and a middle semiconductor region above the lower semiconductor structure. The middle semiconductor region has a second-type impurity (e.g., N-type) complementary to the first-type impurity.

[0010] This method protects a portion of the middle semiconductor structure using a sacrificial mask that is positioned over a center of the middle semiconductor region and silicides exposed portions of the middle semiconductor structure. The siliciding process leaves a non-silicided portion of the middle semiconductor structure over the center of the middle semiconductor region.

[0011] Next, this process forms an upper semiconductor structure opening through a center of the non-silicided portion of the middle semiconductor region, forms spacers in the upper semiconductor structure opening, and forms a T-shaped upper semiconductor structure in the upper semiconductor structure opening. The spacers separate the upper semiconductor structure from silicided portions of the middle semiconductor region.

[0012] The NPN or PNP transistor produced by this process in-

cludes a lower semiconductor structure having a first-type impurity, a middle semiconductor region above the lower semiconductor structure (the middle semiconductor region has a second-type impurity complementary to the first-type impurity), and a T-shaped upper semiconductor structure above the middle semiconductor region. The upper semiconductor structure also has the first-type impurity.

[0013] These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

BRIEF DESCRIPTION OF DRAWINGS

[0014] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0015] Figure 1 is a schematic diagram of a partially completed structure according to the invention;

[0016] Figure 2 is a schematic diagram of a partially completed structure according to the invention;

[0017] Figure 3 is a schematic diagram of a partially completed structure according to the invention;

[0018] Figure 4 is a schematic diagram of a partially completed structure according to the invention;

[0019] Figure 5 is a schematic diagram of a partially completed structure according to the invention;

[0020] Figure 6 is a schematic diagram of a partially completed structure according to the invention;

[0021] Figure 7 is a schematic diagram of a partially completed structure according to the invention;

[0022] Figure 8 is a schematic diagram of a partially completed structure according to the invention;

[0023] Figure 9 is a schematic diagram of a partially completed structure according to the invention;

[0024] Figure 10 is a schematic diagram of a partially completed structure according to the invention;

[0025] Figure 11 is a schematic diagram of a partially completed structure according to the invention;

[0026] Figure 12 is a schematic diagram of a partially completed

structure according to the invention;

[0027] Figure 13 is a schematic diagram of a partially completed structure according to the invention; and

[0028] Figure 14 is a schematic diagram of a partially completed structure according to the invention.

DETAILED DESCRIPTION

[0029] The present invention and the various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0030] As mentioned above, the resistance of the base in bipolar PNP/NPN devices in bipolar complementary metal oxide semiconductor (BiCMOS) technologies or in bipolar-only

technologies dramatically affects the performance of the devices. The invention described below provides a silicide layer adjacent the intrinsic base using a unique structure and methodology to address these issues. More specifically, as shown in Figures 1-8, the invention discloses a method of making bipolar complementary metal oxide semiconductor (BiCMOS) devices and PNP/NPN transistors.

[0031] As shown in Figure 1, the invention forms an intrinsic base layer 116, 118 above a substrate layer 110 that includes a collector 112, and shallow trench isolation (STI) regions 114 (such as SiO_2 or other similar isolation materials) formed adjacent the collector 112. Region 116 is above STI region 114 and is polycrystalline. Region 118 is above region 112 and is single crystalline. There is a facet between region 116 and 118 known to those skilled in the art. A raised extrinsic base 200, 202 is formed above the intrinsic base layer 116, 118 through an epitaxial growth process. The epitaxial growth process maintains the crystal structure of the underlying intrinsic base 118 in the extrinsic regions 202. Therefore, if the intrinsic base 118 is single crystal silicon, the extrinsic base 202 will also be single crystal silicon. Note that the intrinsic base 118 portion that is grown over the collector 112 sees a faster

growth rate than the polysilicon 116 that is grown over the insulator 114. Therefore, the single crystal intrinsic base 118 is raised above the corresponding polysilicon regions 116.

[0032] In addition, a landing pad insulator 120 is patterned on the center of the intrinsic base 118. The insulator 120 can comprise any conventional insulator such as silicon dioxide, silicon nitride, etc., or a stack of the combinations of these layers. The film stack can also have a poly or amorphous Si layer as the topmost layer. Further, the insulator 120 is narrower than the intrinsic base 118 width, but wider than the opening that will be formed for the emitter at later steps.

[0033] As shown in Figure 2, a silicon layer that is the extrinsic base 200, 202 is formed above region 116 during intrinsic base growth. This silicon layer 200 is also formed in an epitaxial growth process. Therefore, regions of the extrinsic base 200 grown above the polysilicon intrinsic base 116 will comprise additional polysilicon. The regions of the extrinsic base 202 grown above the single crystal silicon 118 will also comprise single crystal silicon. To the contrary, the region of the extrinsic base 204 grown above the insulator 120 comprises polysilicon. Note that

the width of the insulator 120 determines the width of the raised polysilicon portion 204 of the extrinsic base.

[0034] The invention protects a portion of the extrinsic base 200 using a sacrificial mask 206 that is patterned over the center of the extrinsic base 204. This mask layer can be an oxide layer, a nitride layer, an oxynitride layer, or a combination of these insulating layers. Figure 2 illustrates the deposition of the sacrificial mask 206 and Figure 3 illustrates the mask 206 after patterning.

[0035] As shown Figure 4, the invention silicides exposed portions of the extrinsic base 200, 202 that are not protected by the sacrificial mask 206. More specifically, the invention sputters metals such as cobalt, titanium, nickel, niobium, etc. over the structure and heats the structure to form the silicide 400. This layer 400 is actually a salicide because it is self-aligned. This siliciding process leaves a non-silicided portion of the extrinsic base 204 over the center of the intrinsic base 118 and over regions on the wafer other than the extrinsic base regions of the bipolar npn or pnp devices. This process also consumes a portion of the silicon 200, 202, thereby forming the silicide 400 horizontally (laterally) adjacent to the non-silicided silicon 204 and raising region 204 further with respect to regions

200, 202. The excessive metal and mask 206 is then removed.

[0036] Before forming the emitter opening, as shown in Figure 5, the invention forms an insulator layer 500 (e.g., TEOS, etc.) above the extrinsic base. Then, as shown in Figure 6, the invention etches an opening 600 for the emitter. Thus, this process forms the emitter opening 600 through the center of the non-silicided portion of the extrinsic base 204 down to the insulator 120.

[0037] Next, as shown in Figure 7, the invention forms spacers 700 (e.g., nitride, etc.) in the emitter opening 600 along the sidewalls of the non-silicided silicon 204. Next, the emitter opening 600 is extended through the insulator 204 to expose the upper portion of the intrinsic base 118. Following this, the invention forms an emitter 800 in the emitter opening 600. After further processing steps known to those skilled in the art, the final emitter has T-shape. One feature of this aspect of the invention is that the non-silicided portion of the extrinsic base 204 and the spacers 700 separate the emitter 800 from the silicide regions 400.

[0038] This produces a bipolar device that has a collector 112, an intrinsic base 118 above the collector 112, a raised ex-

trinsic base 202 above and on the sides of the intrinsic base, and an emitter 800 above the intrinsic base 118. The emitter 800 has a T-shape with a lower section and an upper section that is wider than the lower section. The spacers 700 are adjacent the lower section of the emitter and beneath the upper section of the emitter, and the silicided portion of the extrinsic base 202 is adjacent the spacers and beneath the upper section of the emitter.

[0039] This structure includes a dielectric structure 120 over the base 118 and beneath the spacers 700, where the base 118 is wider than the dielectric structure 120. The spacers 700 separate the emitter 800 from the silicide and comprise insulators. Because it is self-aligned, the silicide is called a salicide.

[0040] While the foregoing process is described with respect to an NPN device in a BiCMOS technology or a bipolar-only technology, it is equally applicable to a PNP device. In such a structure, Figures 1-8 illustrate a lower semiconductor structure 112 having a first-type impurity, a middle semiconductor region 118 above the lower semiconductor structure 112 (the middle semiconductor region has a second-type impurity complementary to the first-type impurity), and a T-shaped upper semiconductor

structure 800 above the middle semiconductor region 112, 118. The upper semiconductor structure 800 also has the first-type impurity. This structure also includes spacers 700 adjacent the upper semiconductor structure 800. Again, one feature of this structure is that the non-silicided portion of the middle semiconductor region 204 and the spacers 700 separate the upper semiconductor region 800 from the silicide regions 400.

[0041] Figures 9-14 illustrate an additional embodiment of the invention that is somewhat similar to the previous embodiment. The same features discussed above are identified with the same reference numbers and a redundant discussion of the same is avoided. Therefore, only the differences between the previous embodiment and the additional embodiment are discussed herein. More specifically, as shown in Figure 9, this embodiment omits the need to utilize the mask 206 while performing the silicide process. Therefore, the silicide layer 900 is continuous across all portions of the extrinsic base 200, 202, 204. Figure 10 illustrates the formation of the emitter opening 600. Figure 11 illustrates the formation of the spacers 700. Figure 12 illustrates the extension of the emitter opening 600 through the insulator 120. Figure 13 illustrates the depo-

sition of the emitter material 800 and Figure 14 illustrates the patterning of the emitter material 800 to form the T-shaped emitter.

[0042] Both embodiments discussed above reduce device resistance by use of the silicide layer beneath the upper portion of the T-shaped emitter 800, which increases device speed. The spacer 700 prevents short circuits to maintain high yield and reliability. The first embodiment shown in Figures 1-8 is more efficient than the second embodiment shown in Figures 9-14; however both embodiments produce the benefits of reduced resistance, without affecting yield.

[0043] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

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Claims

[c1] 1.A bipolar device comprising:
a base;
an emitter above said base, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section;
spacers adjacent said lower section of said emitter and beneath said upper section of said emitter; and
a silicide layer adjacent said spacers and beneath said upper section of said emitter.

[c2] 2.The device in claim 1, further comprising a dielectric structure over said base and beneath said spacers.

[c3] 3.The device in claim 2, wherein said base is wider than said dielectric structure.

[c4] 4.The device in claim 1, wherein said spacers separate said emitter from said silicide.

[c5] 5.The device in claim 1, wherein said base comprises:
an intrinsic base; and
an extrinsic base above said intrinsic base.

[c6] 6.The device in claim 1, wherein said spacers comprise

insulators.

[c7] 7.The device in claim 1, wherein said silicide layer comprises a salicide.

[c8] 8.A transistor device comprising:
a lower semiconductor structure having a first-type impurity;
a middle semiconductor region above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity;
an upper semiconductor structure above said middle semiconductor region, wherein said upper semiconductor structure has a T-shape with a lower section and an upper section that is wider than said lower section;
spacers adjacent said lower section of said upper semiconductor structure and beneath said upper section of said upper semiconductor structure; and
a silicide layer adjacent said spacers and beneath said upper section of said upper semiconductor structure.

[c9] 9.The device in claim 8, further comprising a dielectric structure over said middle semiconductor region and beneath said spacers.

[c10] 10.The device in claim 9, wherein said middle semicon-

ductor region is wider than said dielectric structure.

[c11] 11.The device in claim 8, wherein said spacers separate said upper semiconductor structure from said silicide.

[c12] 12.The device in claim 8, wherein said middle semiconductor region comprises:
an intrinsic middle semiconductor region; and
an extrinsic middle semiconductor region above said intrinsic middle semiconductor region.

[c13] 13.The device in claim 8, wherein said spacers comprise insulators.

[c14] 14.The device in claim 8, wherein said silicide comprises a salicide.

[c15] 15.A method of making a transistor, said method comprising:
forming a extrinsic base above an intrinsic base;
protecting a portion of said extrinsic base using a sacrificial mask that is positioned over a center of said extrinsic base;
siliciding exposed portions of said extrinsic base,
wherein said siliciding process leaves a non-silicided portion over said center of said extrinsic base;
forming an emitter opening through a center of said non-silicided portion of said extrinsic base;

forming spacers in said emitter opening; and
forming an emitter in said emitter opening,
wherein said spacers separate said emitter from silicided portions of said extrinsic base.

[c16] 16.The method in claim 15, further comprising, before forming said extrinsic base:
patterning an insulator over said center of said intrinsic base; and
epitaxially growing said extrinsic base over said insulator and said intrinsic base.

[c17] 17.The method in claim 16, wherein said process of epitaxially growing said extrinsic base grows polysilicon above said insulator and single crystal silicon above the exposed portions of said intrinsic base.

[c18] 18.The method in claim 16, wherein said spacers are formed on said insulator.

[c19] 19.The method in claim 15, wherein said siliciding process forms said silicided portions of said extrinsic base horizontally adjacent to said non-silicided portion.

[c20] 20.The method in claim 15, further comprising, before forming said emitter opening, forming an insulator layer above said extrinsic base, wherein said emitter opening is formed through said insulator layer.

[c21] 21.A method of making a transistor, said method comprising:

forming a lower semiconductor structure having a first-type impurity;

forming a middle semiconductor region above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity;

protecting a portion of said middle semiconductor region using a sacrificial mask that is positioned over a center of said middle semiconductor region;

siliciding exposed portions of said middle semiconductor region, wherein said siliciding process leaves a non-silicided portion over said center of said middle semiconductor region;

forming an upper semiconductor structure opening through a center of said non-silicided portion of said middle semiconductor region;

forming spacers in said upper semiconductor structure opening; and

forming an upper semiconductor structure in said upper semiconductor structure opening,

wherein said spacers separate said upper semiconductor structure from silicided portions of said middle semiconductor region.

[c22] 22.The method in claim 21, further comprising, before forming said middle semiconductor region:
forming a silicon layer over said lower semiconductor regions;
patterning an insulator over said center of said silicon layer; and
epitaxially growing said middle semiconductor region over said insulator and said silicon layer.

[c23] 23.The method in claim 22, wherein said process of epitaxially growing said middle semiconductor region grows polysilicon above said insulator and single crystal silicon above the exposed portions of said silicon layer.

[c24] 24.The method in claim 21, wherein said spacers are formed on said insulator.

[c25] 25.The method in claim 21, wherein said siliciding process forms said silicided portions of said middle semiconductor region horizontally adjacent to said non-silicided portion.

[c26] 26.The method in claim 21, further comprising, before forming said upper semiconductor structure opening, forming an insulator layer above said middle semiconductor region, wherein said upper semiconductor structure opening is formed through said insulator layer.

[c27] 27.A method of making a bipolar complementary metal oxide semiconductor (BiCMOS) device, said method comprising:
forming a collector;
forming shallow trench isolation regions adjacent said collector;
forming an intrinsic base above said collector;
forming a raised extrinsic base above said intrinsic base;
protecting a portion of said extrinsic base using a sacrificial mask that is positioned over a center of said extrinsic base;
siliciding exposed portions of said extrinsic base,
wherein said siliciding process leaves a non-silicided portion over said center of said extrinsic base;
forming an emitter opening through a center of said non-silicided portion of said extrinsic base;
forming spacers in said emitter opening; and
forming an emitter in said emitter opening,
wherein said spacers separate said emitter from silicided portions of said extrinsic base.

[c28] 28.The method in claim 27, further comprising, before forming said extrinsic base:
patterning an insulator over said center of said intrinsic base; and
epitaxially growing said extrinsic base over said insulator

and said instinsic base.

[c29] 29.The method in claim 28, wherein said process of epitaxially growing said extrinsic base grows polysilicon above said insulator and single crystal silicon above the exposed portions of said intrinsic base.

[c30] 30.The method in claim 27, wherein said siliciding process forms said silicided portions of said extrinsic base horizontally adjacent to said non-silicided portion.

[c31] 31.The method in claim 27, wherein said spacers are formed on said insulator.

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A METHOD OF BASE FORMATION IN A BICMOS PROCESS

Abstract

Disclosed is a bipolar complementary metal oxide semiconductor (BiCMOS) or NPN/PNP device that has a collector, an intrinsic base above the collector, shallow trench isolation regions adjacent the collector, a raised extrinsic base above the intrinsic base, a T-shaped emitter above the extrinsic base, spacers adjacent the emitter, and a silicide layer that is separated from the emitter by the spacers.

FIG. 1

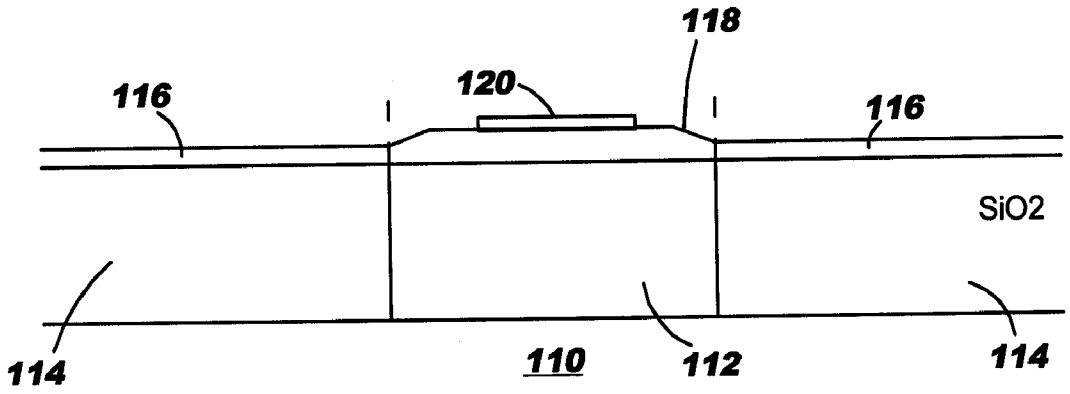

FIG. 2

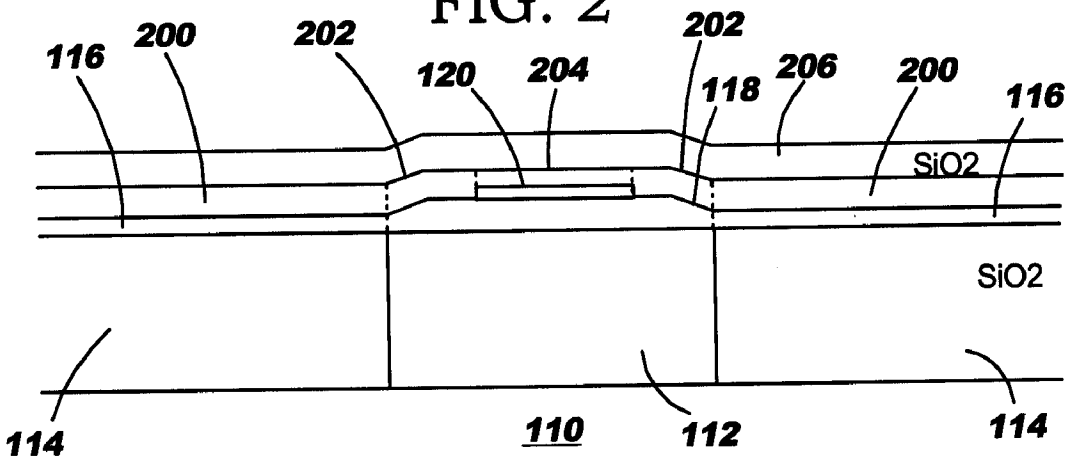

FIG. 3

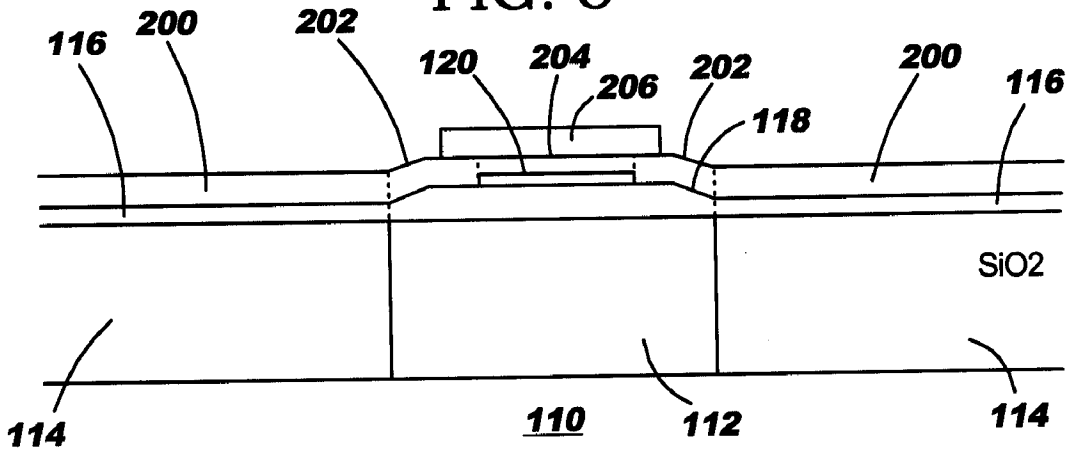

FIG. 4

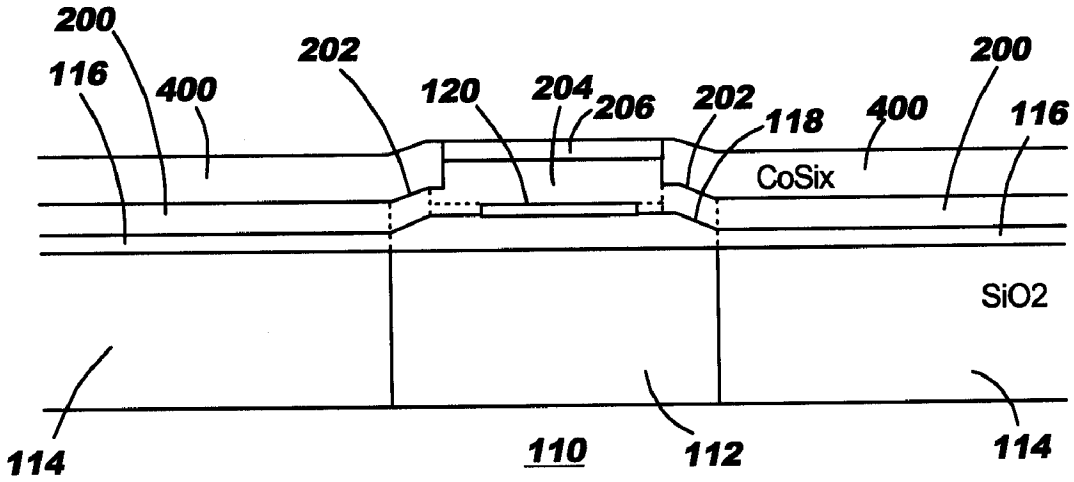
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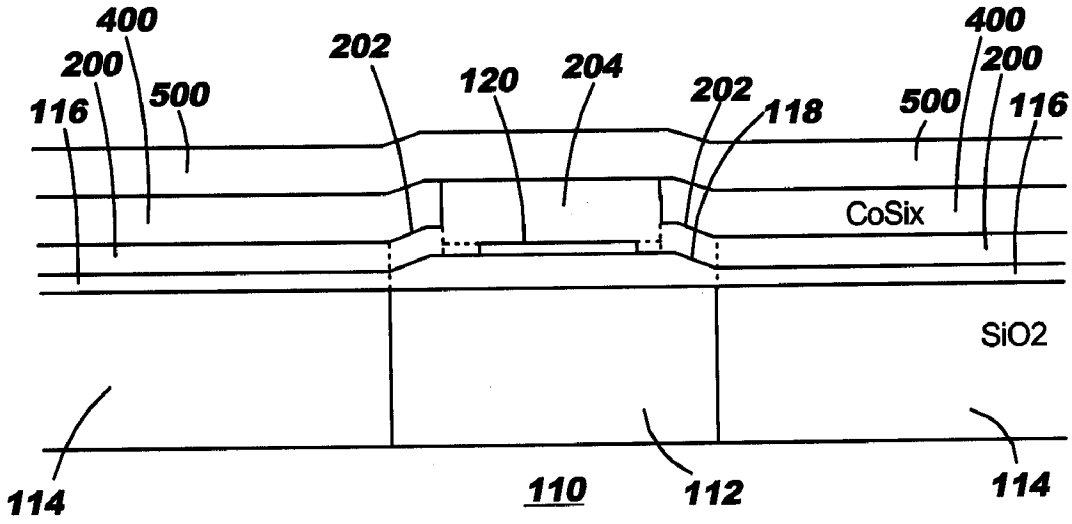
FIG. 5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114

FIG. 6

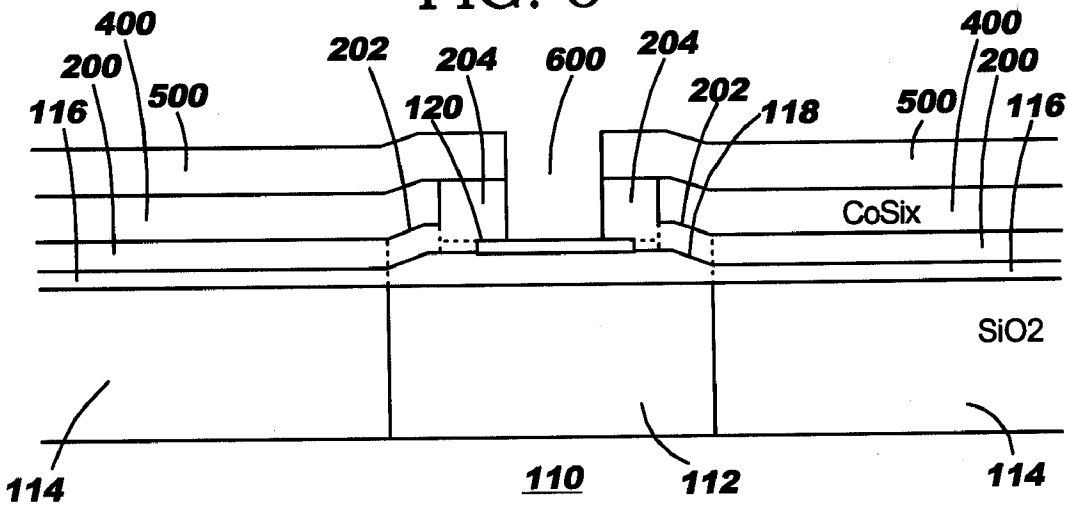


FIG. 7

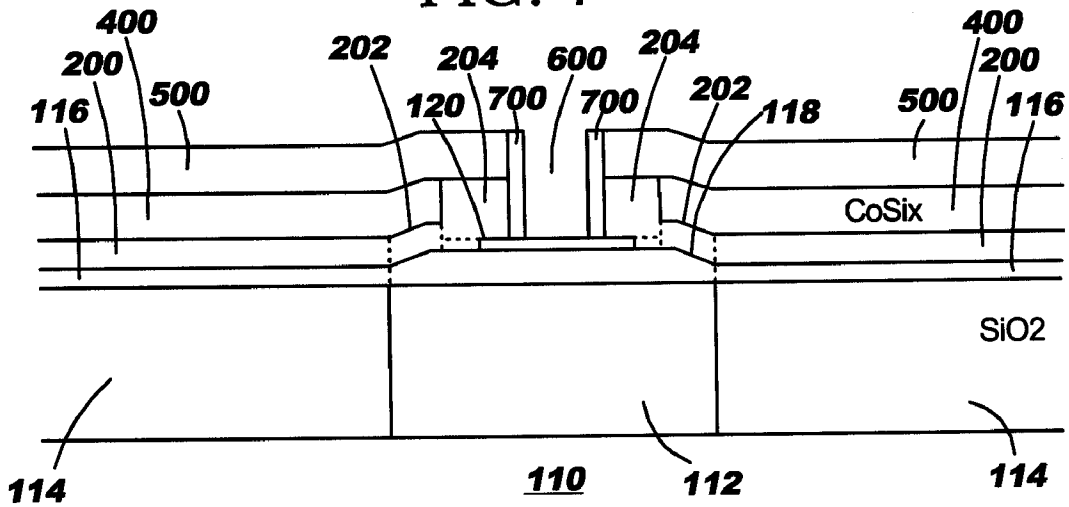


FIG. 8

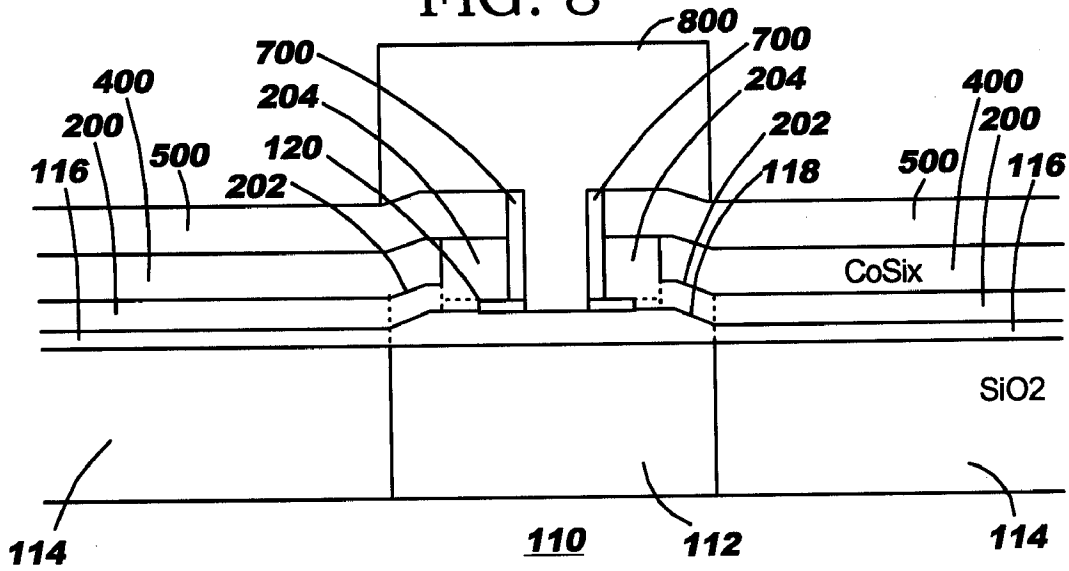


FIG. 9

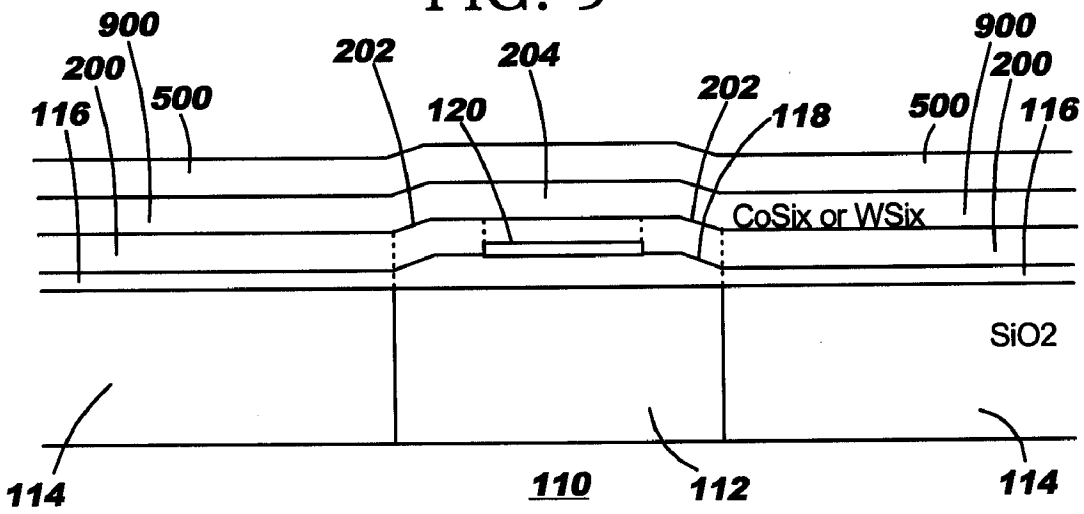


FIG. 10

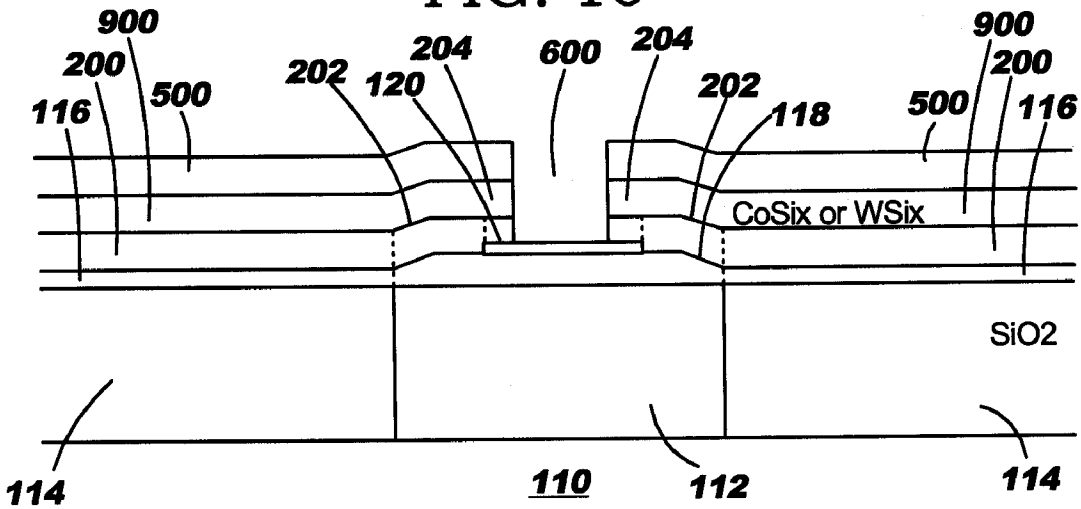


FIG. 11

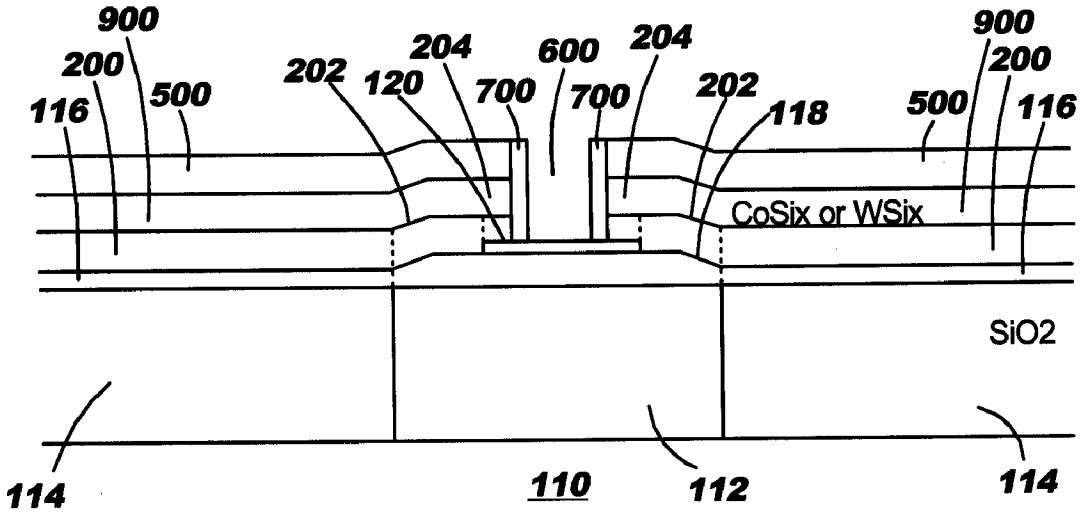


FIG. 12

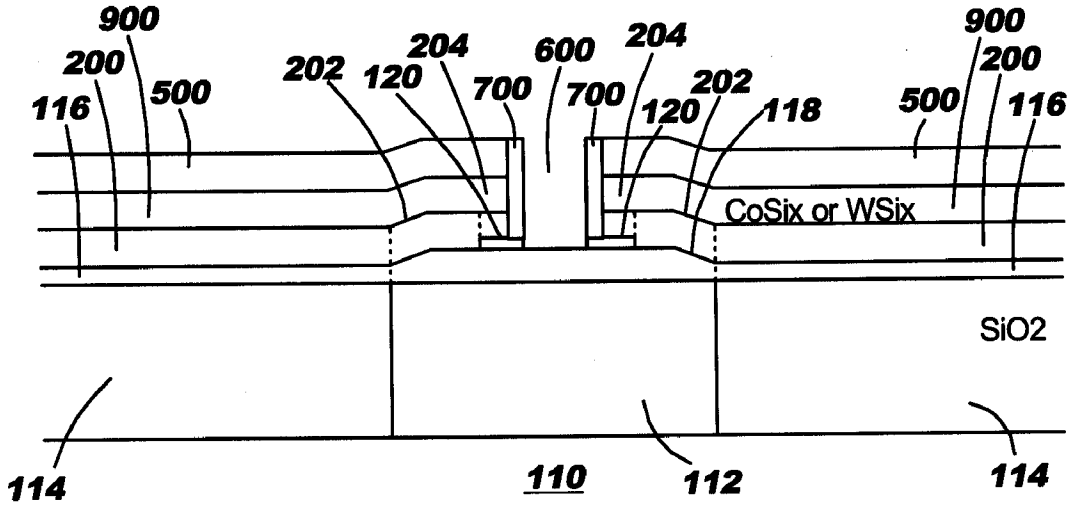


FIG. 13

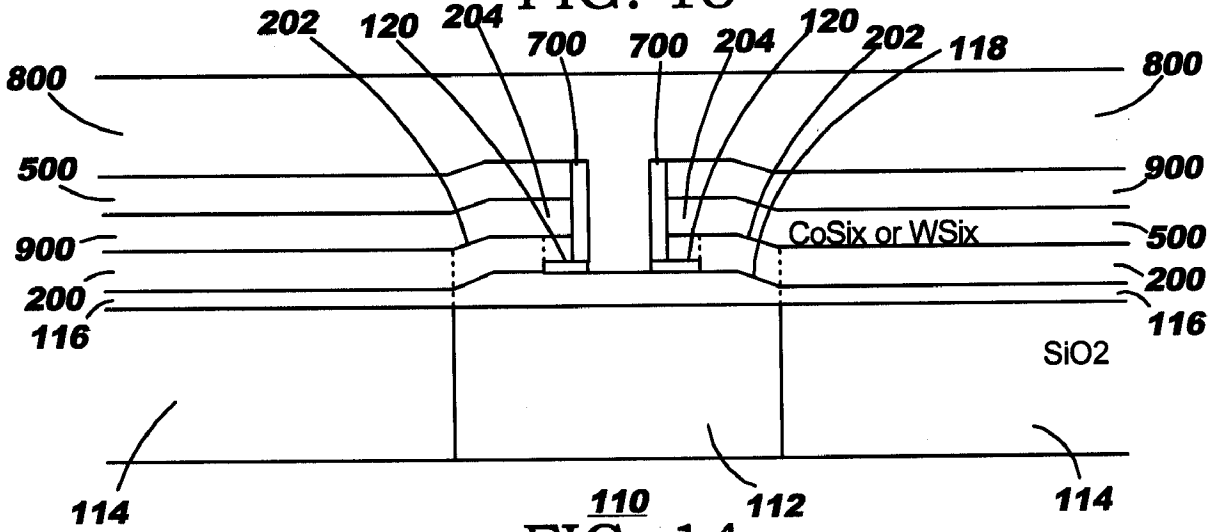
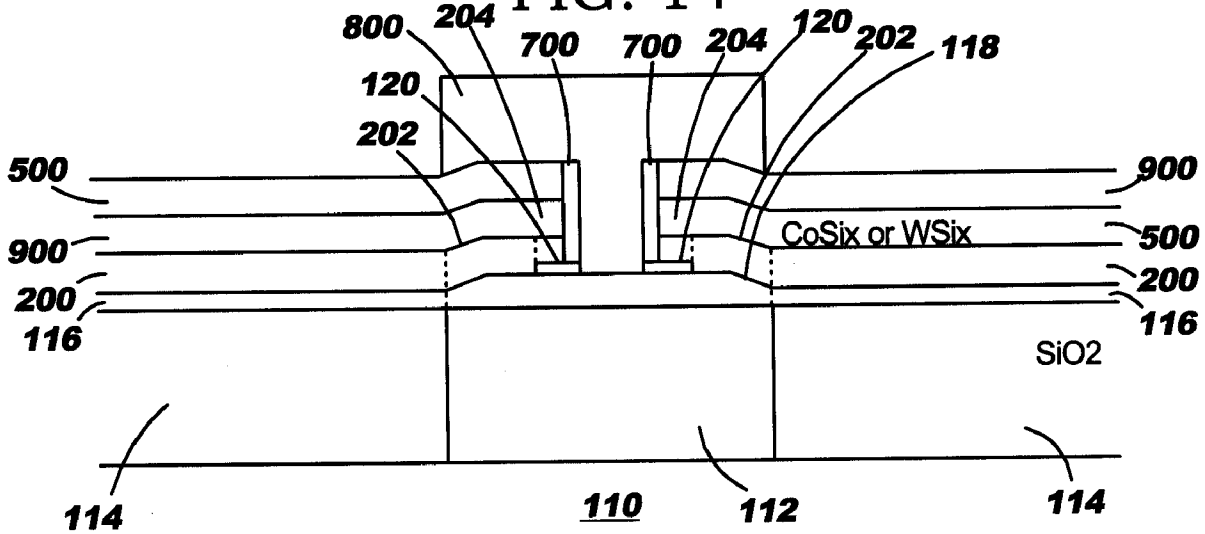


FIG. 14



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **A METHOD OF BASE FORMATION IN A BICMOS PROCESS** the specification of which:
(check one)

☒ is attached hereto.
☐ was filed on _____, as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the attorneys and/or agents listed under Customer No. 29154 to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Send all correspondence to: **McGinn & Gibb, PLLC, 2568-A Riva Road, Suite 304, Annapolis, Maryland 21401. Customer No. 29154**

Telephone calls should be directed to Frederick W. Gibb, III, McGinn & Gibb, PLLC at (410) 573-1545.

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